LOW POWER SCALABLE, HIGH PERFORMANCE VOLATILE MRAM BASED FPGA

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Abstract

In this paper, we propose a new structure of FPGA based on Low Power MRAM technology; we name it LP-MFPGA (magnetic FPGA). FPGA based on SRAM technology has been developed in the last years, because of its high speed and near limitless number of reprogramming, however SRAM is volatile thereby the configuration information and the intermediate data will be lost when power is turned off. By using MTJs (magnetic tunnel junction) as the storage elements of FPGA, we can realize the non-volatility of FPGA, and then we will not need the external memory. In our simulation, the start-up time of circuit can be decreased up to some hundred pico seconds. Except for the rapid start-up time, we can also configure the algorithm and logic function of the FPGA circuit very simply and rapidly. The other advantage of using LP-MRAM technology is that we will not enlarge the circuit surface, because the storage element MTJs are on the semiconductor surface. The proposed cell is dynamically reconfigurable in the background, which makes it a proper alternative to replace the SRAM cells of conventional field-programmable gate arrays (FPGAs) for the development of NV-FPGAs .In this design the cache memory architecture allows to change the memory organization and size of its memory by using a cache size controller unit and way controller unit, to improve the processor performance and reduces the energy consumption, and using all available memory size for all possible organization that can be selected. The results show the simulation of the design. This design is synthesized using (Xilinx ISE Design Suite 12.1) and simulated using (Xilinx ISim simulator).

Introduction

Engineering education at Universities are always suffering from the mismatches between rapidly advancing technology at the side of industry and slowly evolving course materials at the side of University. In the major of computer science and computer engineering, such mismatches seem to be more frequently observed than other science and technology department since the IT technologies have been advanced faster than others. To solve the IT education problems, IEEE Computer Education Society and other IT related society have worked on the education issues from few decade ago. In a current commercial computing system, many core processors are major products of many chip manufacturing vendors (e.g., Intel, AMD, nVidia) [1, 2, 3, 4]. Quad or hexa-core processors are not only available for high-performance computing but also available for general computing in desktop PC computers. Moreover, those many core systems are also used in mobile phones. However, in the undergraduate course work of computer science (CS) or computer engineering (CE), there is not yet enough classes for many core system architecture and

programming. In consequence, a many core processor is one topic of such mismatches paradigm happen between academia and industry. Recently, there have been parallel programming classes in which the lectures on practical CUDA or Open CL parallel programming languages are provided [5, 6]. However, it seems that there is no enough class on the many core processor at the viewpoint of a computer architecture. Some advanced chapters of textbooks in computer architecture classes cover the theoretical points of modern high-performance many core processor architectures, but they do not provide actual design or In the literatures of CS and CE educations, there have been many work so far with long history for supporting teaching materials and for establishing course contents that are efficiently deliverable to CS and CE majored university students with better understanding [9]. In [10], the authors have develop a computer-aided teaching package for teaching a processor architecture. The CAT is composed of an assembler and a graphics simulator. In the study, a simple Z80 model is used as a processor model. Similar to [10], a simple processor simulator has been developed as a teaching tool for first-year undergraduates [11]. As a program run on the simulator, the tool shows a snapshot of the processor internals such as register values and program counter. In [12], simple micro-architectures are used as a processor education model for first-year students of computer science with a graphic tool that visualize the operations of the micro-architectures. The authors in [13] have presented a graphical and interactive tools for reduced instruction set computer processor and memory simulator. Through those visualizing tools, undergraduate students can actively learn theoretical concepts covered in computer architecture classes. It is a unique feature of [13] that the simulator can be configured into processors of having many different levels of complexity from a simple processor without caches or pipelines to a highly complex one with caches and superscalar execution. The core idea behind [10, 11, 12, 13] is supporting visualization tools for better understanding of computer architecture operations. In addition to [10, 11, 12, 13], many of similar visualization approaches have been performed so far in the computer science education society. Another research trend of the processor education in CS / CE is employing an FPGA devices. The programmability of the FPGA is a very fascinating feature in processor design educations because students can make real working processor chip by downloading their designs to the FPGA as opposed to just experimenting software-based simulations. Furthermore, unlike ASIC designs that require at least few months for their implementations, the FPGA device provide a quick verification/test cycle and easy modification capability. Consequently, students can experience all the process of designing a actual product by working on designing, implementing, testing, and debugging processors using a commercial FPGA development boards [14]. Many educational purpose FPGA development boards are available at the University Programs provided by main FPGA chip vendors such as Altera and Xilinx [15, 16]. In [17, 18, 19, 20], an FPGA device has been used as their educational teaching platforms for demonstrating real working processor to students. In [21], the authors have discussed some usage of a FPGA device in teaching processor design class. Most importantly, students can have much motivation toward their learning for computer architecture because developing a real working processor can be a unique experiences. Our goal of work is to provide the educational processor architecture model that follows the recent trend of microprocessor market so that students can feel much higher motivation for their learning.

Problem Identification

Indeed, from the 1990s, the researchers concentrated on innovation and the implementation of a new design: "co-design". However, until the end of the design of dedicated systems is not implemented than on printed circuit boards. Today, the technological development of Submicron with an integration rate of more than one million of transistors has opened the door to the implementation of these systems on a single Chip. This new generation of embedded systems (SoC: "System on Chip") allows to master problems even more complex due to the fact that with a single chip performance (MIPS or FLOPS) higher than those that can be realized with a card. A key phase in the design of SoCs is integration of IP ("Intellectual Properties") blocks that makes operation difficult and expensive in design time. Few studies have been interested in this problem of synthesis communication interface. The constant need for better, faster and more power-efficient electronic systems, has stimulated the need for innovation in every design level. For years, engineers have been pushing the boundaries of Synchronous design, inventing ingenious ways to meet the requirements posed by the electronics industry. Recent years though, have seen an increased focus on Self – Timed system design as an alternative. This paper is a technical report detailing the design of an Asynchronous Memory Controller module.

Existing Work

The dynamic memory controller plays an important role in system-on-a-chip (SoC) designs to provide enough memory bandwidth through external memory for DSP and multi-media processing. As the multimedia applications are growing rapidly past a decade. The applications of multi-media for processing high resolution video, data and audio sequences are known to require a high speed and high-density memory port. The memory is required for data storage in real time applications, the memory controllers support DDR3/DDR2/DDR/SDRAM memories and it can be configured according to their requirements. In spite much research on performance improvement, the external memory performance is lagging. Hence the memory controller is essential. The proposed architecture of multiport memory controller is designed for flexible communication between the master and the slave ports and also the communication speed is increased as the design contains a number of buffers for, and also embedded memory for configuration storage and an arbiter including round robin scheduling scheme for scheduling the read/write accesses. The design technique provides flexible systems and independent from other system architecture. The design is modelled in Altera and the read/write simulation results are acquired in Modelsim 6.6a using an external DDR3 SDRAM memory.

Lerroelectric RAM history

The development of FRAM dates back to the early days of semiconductor technology. The idea was first proposed in 1952, but it took many years before the idea started to be developed properly as the technologies required to implement it did not exist. Some work on the technology was started in the 1980s, and then in the early 1990s a part of NASA undertook work into the technology for detecting UV radiation pulses. However around 1999 the first devices were produced and since then

companies including Ramtron, Fujitsu, Texas Instruments, Samsung, Matsushita, Infineon and other have been using the technology.

FRAM usage

Currently ferroelectric RAM is not as widely used as many of the more established technologies including DRAM and Flash. These technologies have become well entrenched and their use is widespread. As developers often tend to rely on trusted technologies that are guaranteed to deliver the performance they require, they are often reluctant to use technologies like FRAM that are not guaranteed to deliver. Also issues like memory density that limit the size of memory available have caused them not to be so widely used. However FRAM technology is now being embedded into chips using CMOS technology to enable MCUs to have their own FRAM memories. This requires fewer stages than the number required for incorporating Flash memory onto MCU chips, thereby providing some significant cost reductions.

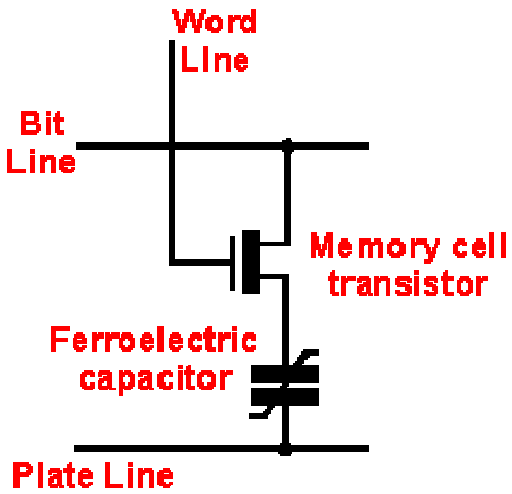

Figure 1 Basic Ferroelectric Memory Cell

A further advantage, apart from the non-volatile nature of the memory is its very low power consumption which lends itself admirably to use within MCUs where power consumption is often a key issue.

Proposed Hierarchical Test Integration Architecture

The proposed hierarchical test integration architecture for 3D ICs. The test integration architecture consists of two control interfaces, the master control interface (MCI) and the slave control interface (SCI), for controlling DFT circuits within dies and handling test operations of a 3D IC. If a 3D IC has N dies, one MCI is integrated with the master die (i.e., the bottom die) and each die of N − 1 non-bottom dies has an individual SCI. Furthermore, if a 3D IC with hierarchical designs, the number of dies with MCI in the 3D IC is larger than 2. As Fig. 1(a) shows, the TCK, TDI, TMS, and TDO are the test pads of each die. The TDITD or TDITU in a layer denotes the TDI

port connected to the TSV in which the test data is transported from the lower layer or higher layer, respectively. The TDOTD or TDOTU denotes the TDO port connected to the TSV in which the test data is sent to the lower layer or higher layer, respectively. When the board-level test is performed, only the MCI in the bottom die is enabled and the MCIs and SCIs in non-bottom dies are idled. When the 3D IC testing is considered, the instructions for the MCIs and SCIs are loaded in a hierarchical way. After the instructions in the test interfaces are loaded, the DFT circuits in the 3D IC can be accordingly controlled. Detailed test control flow will be introduced later.Clearly, the test interfaces transport the test data through the serial TDI-TDO path. Therefore, the parallel test data transportation mechanism should be implemented to reduce the testing time of the 3D IC. As Fig. 1(a) shows, an inter-die test access mechanism (TAM) can be implemented for test data transportation among the dies of a 3D IC. TAM architectures proposed for SOC testing also can be used to implement the inter-die TAM. Hereafter, we thus do not cover the design of inter-die TAM.

Result and Discussion

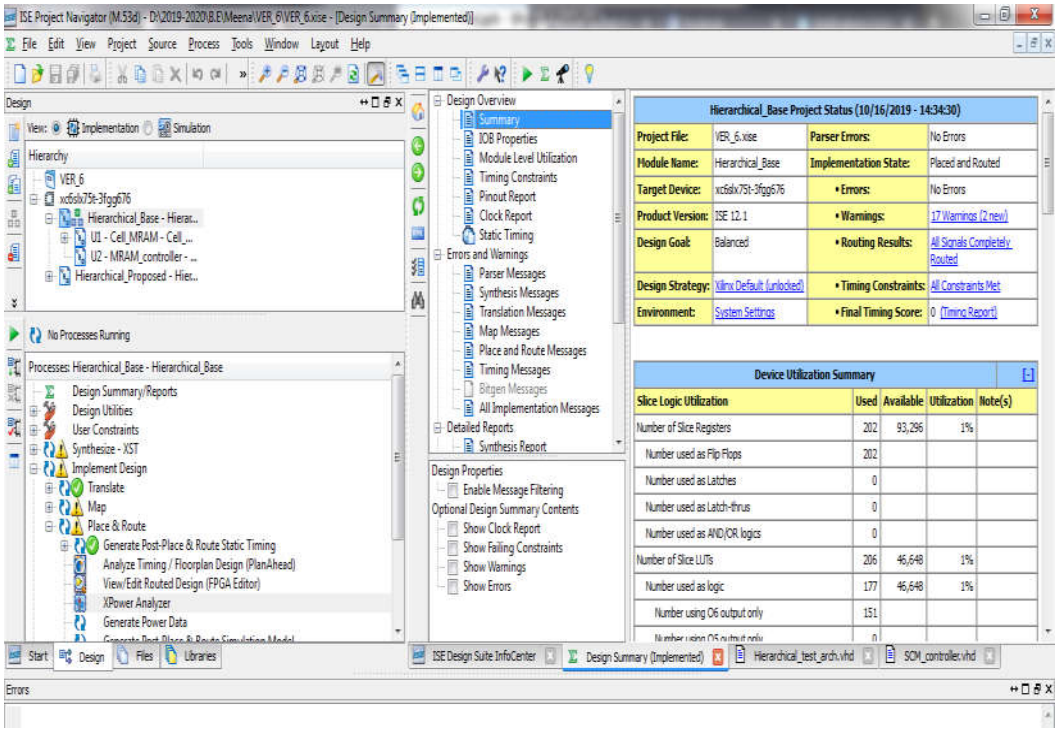

Figure 2 Base Area @ 202 Slices

The Area analysis of Base system is shown in above fig 2. This analysis mainly concentrated on the total number of slice registers and the slice LUTs in the entire system and the number of slice registers and the slice LUTs used to obtain the output. Hence, the available numbers of slice registers are 93,296 and the used numbers of slice registers are 202. The available slice LUTs are 46,560 and the used number of slice LUTs are 202. The utilization of slice register is 1% and the slice LUT is 4%.

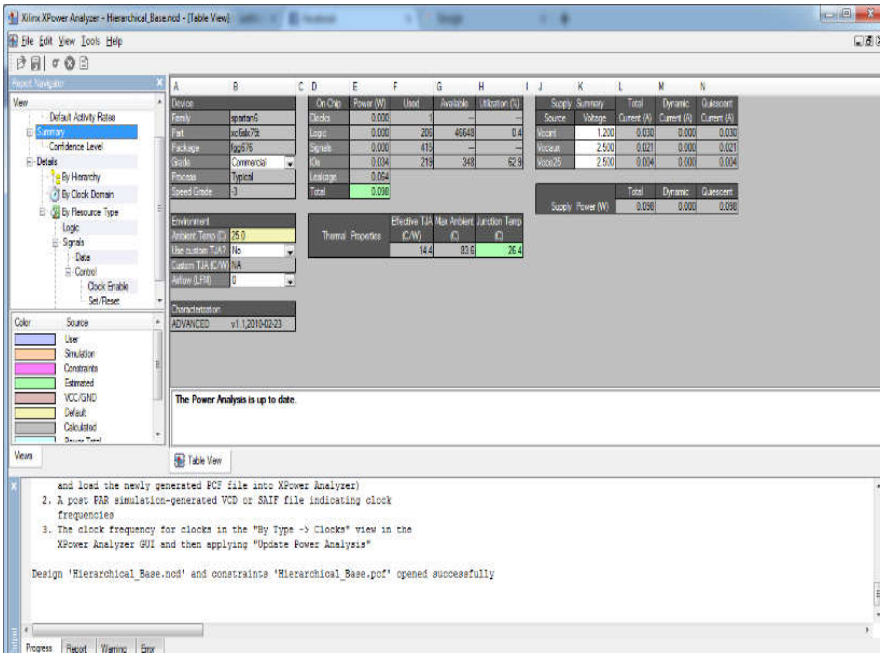

Figure 3 Base Power @ 63.3%(0.064W)

The Power analysis of Base System is shown in above fig 3. This analysis mainly concentrated on the number IOs in the entire system to obtain the output. In the entire system, the available numbers of IOs are 206 and the IOs used to obtain the output are 348. The utilization of power is 63.3%(0.064W).

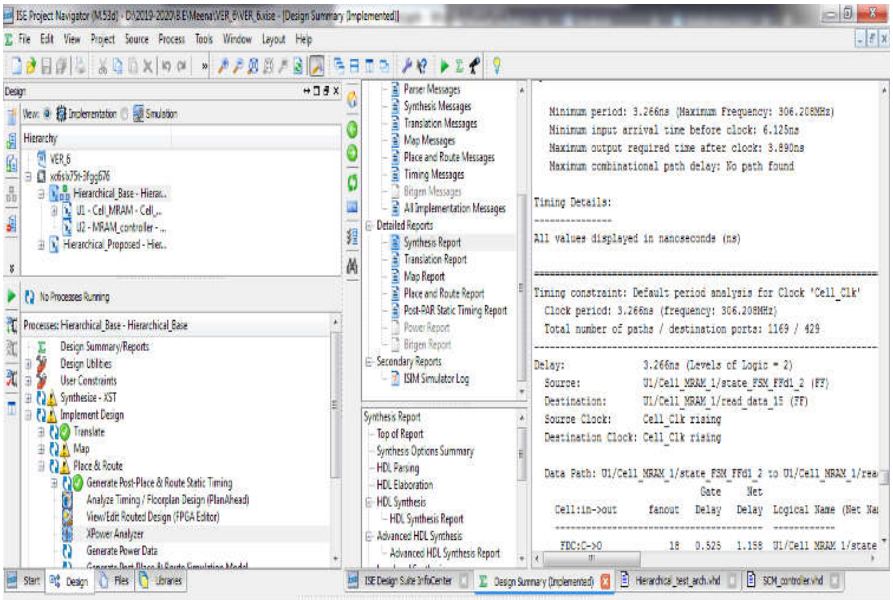

Figure 4 Base Speed @ 306.208MHz

The Speed analysis of Base is shown in the above fig 4. This analysis depends upon the maximum range of frequency. Hence, the maximum range of frequency used to generate the output is 306.202 MHz.

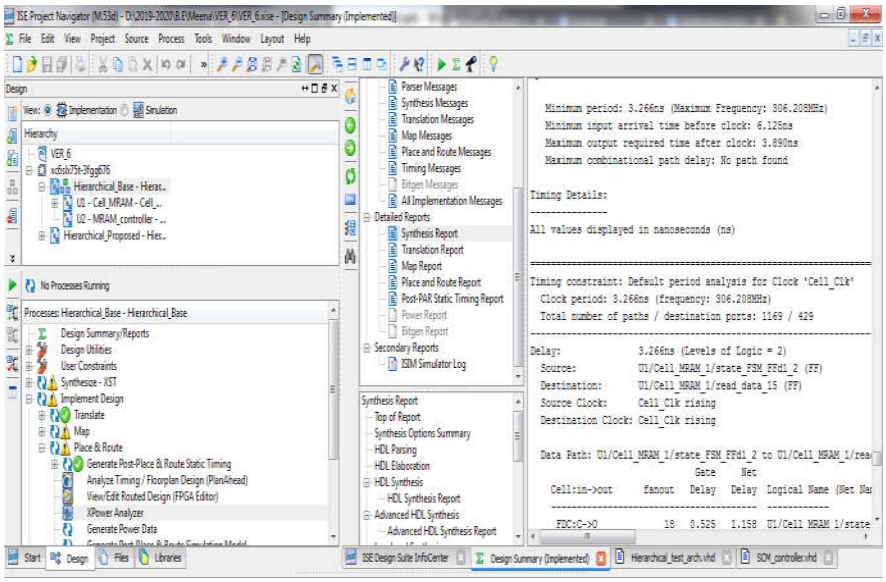

Figure 5 Base Latency @ 3.266ns

The Delay analysis of Base System is shown in above fig 5. The Main concentration of delay analysis is based on the time taken to obtain the output from the time of applying input. Hence, the total time required to XST the completion is 3.266ns.

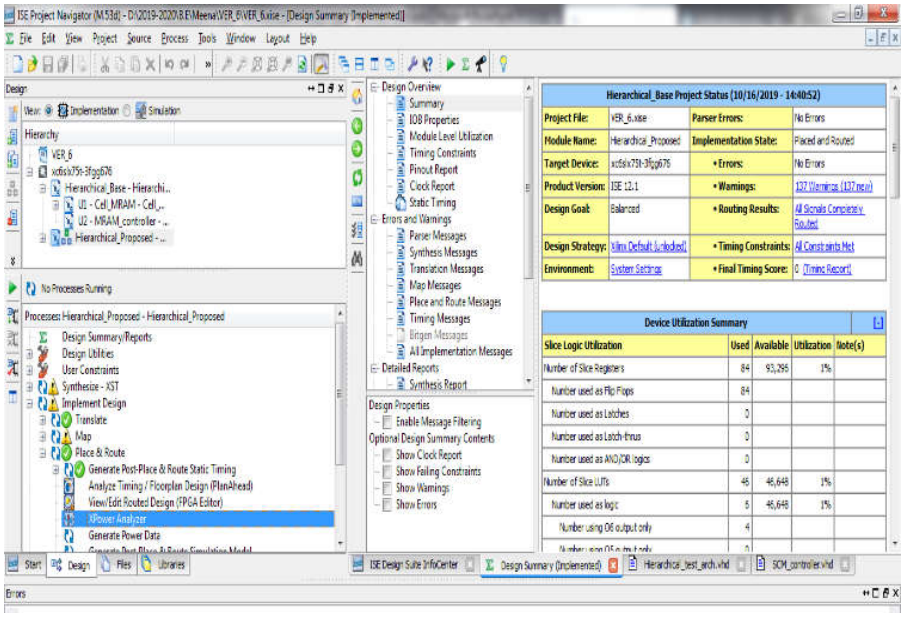

Figure 6 Phase 1 Area @ 84 Slices

The Area analysis of Proposed system is shown in above fig 6. This analysis mainly concentrated on the total number of slice registers and the slice LUTs in the entire system and the number of slice registers and the slice LUTs used to obtain the output. Hence, the available numbers of slice registers are 93,296 and the used numbers of slice registers are 84. The available slice LUTs are 46,645 and the used number of slice LUTs are 84. The utilization of slice register and the slice LUT is 1%.

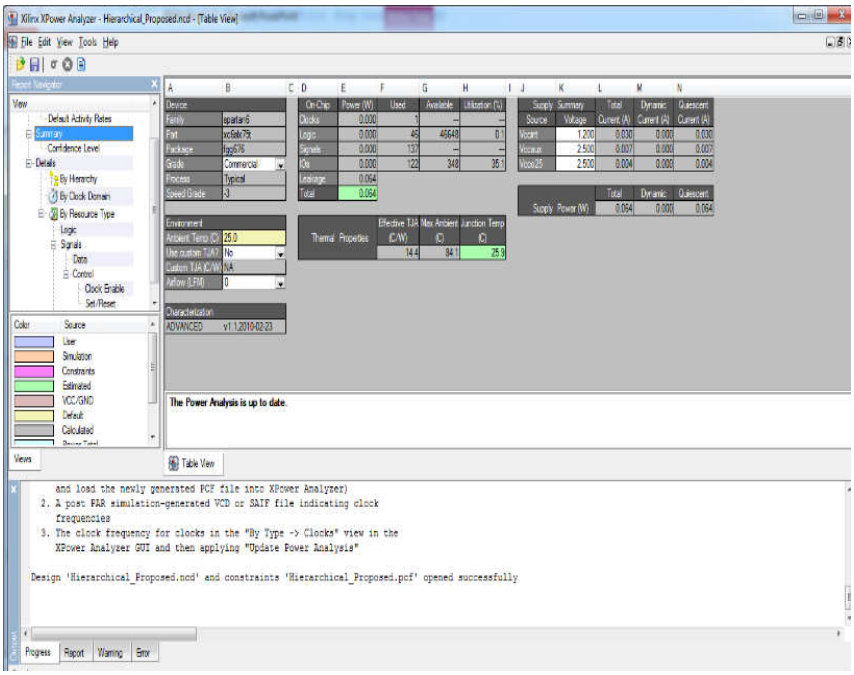

Figure 7 Phase 1 Power @ 35.2% (0.064W)

The Power analysis of Proposed is shown in above fig 7. This analysis mainly concentrated on the number IOs in the entire system to obtain the output. In the entire system, the available numbers of IOs are 46 and the IOs used to obtain the output are 348. T the utilization of power is 35.2%(.064W).

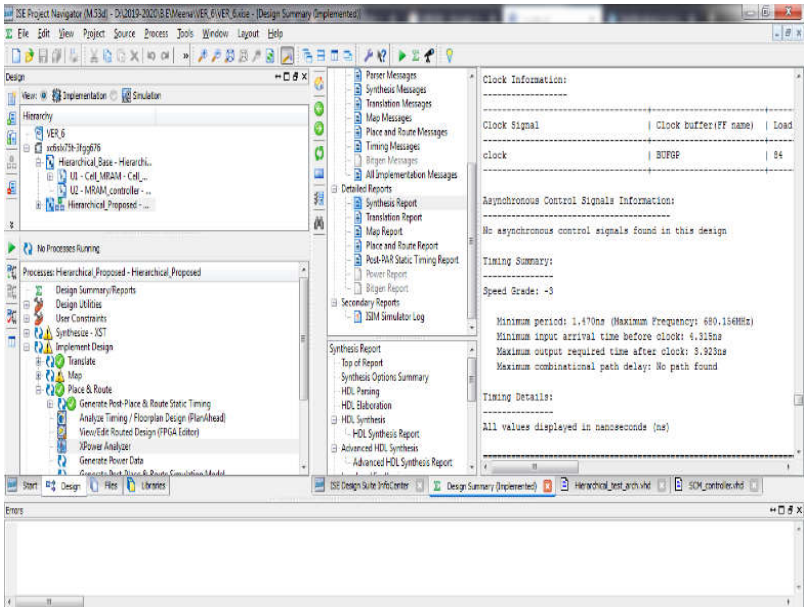

Figure 8 Phase 1 Speed @ 680.156MHz

The Speed analysis of Proposed is shown in the above fig 8. This analysis mainly depends on the maximum range of frequency. Hence, the maximum range of frequency used to generate the output is 680.186MHzMHz.

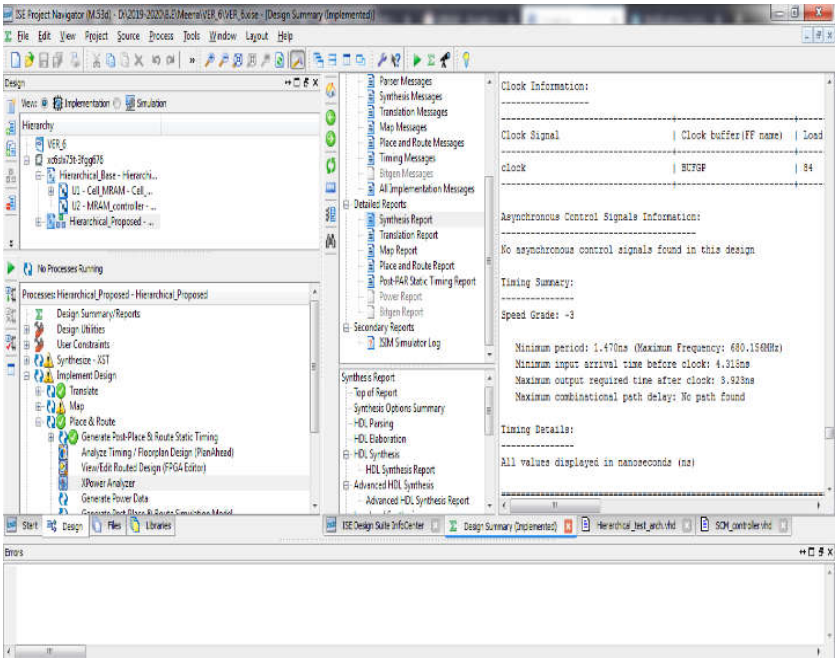

Figure 9 Phase 1 Latency @ 1.470ns

The Delay analysis of proposed system is shown in above fig 9. The Main concentration of delay analysis is based on the time taken to obtain the output from the time of applying input. Hence, the total time required to XST the completion is 1.470ns

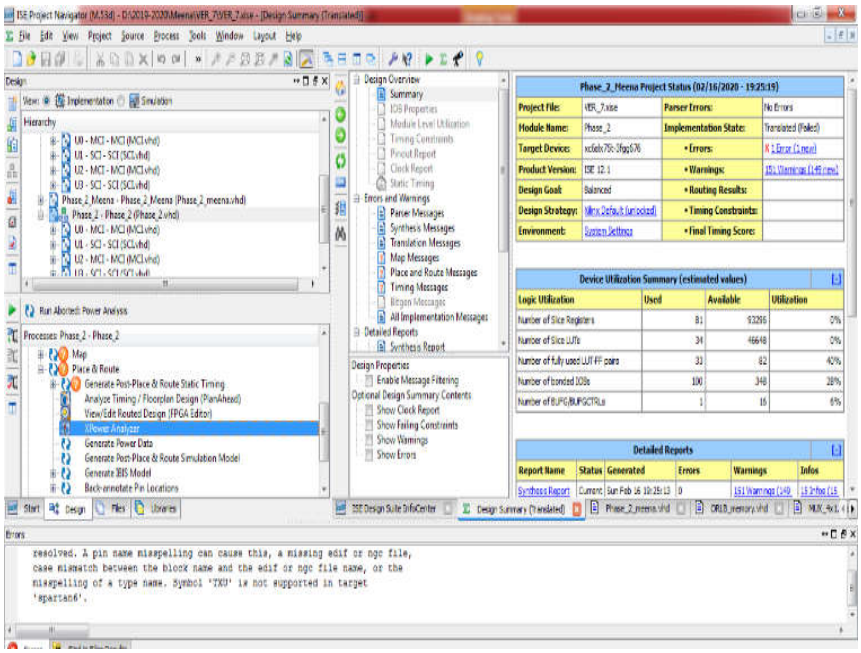

Figure 10 Stand alone Testing based 3d-MRAM Controller with MRAM Area -81

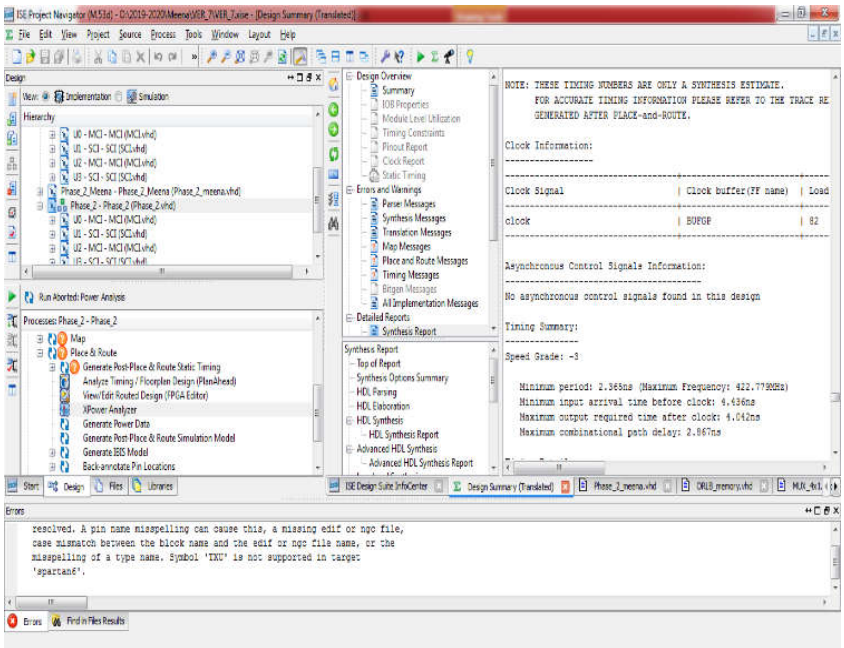

Figure 11 Stand alone Testing based 3d-MRAM Controller with MRAM Speed :422.779MHz

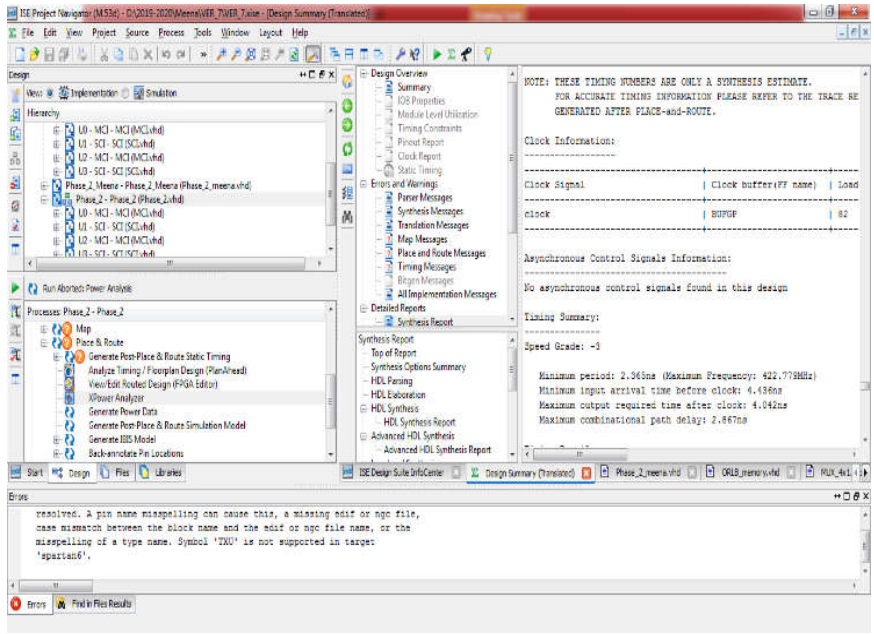

Figure 12 Stand alone Testing based 3d-MRAM Controller with MRAM Latency: 2.365 ns

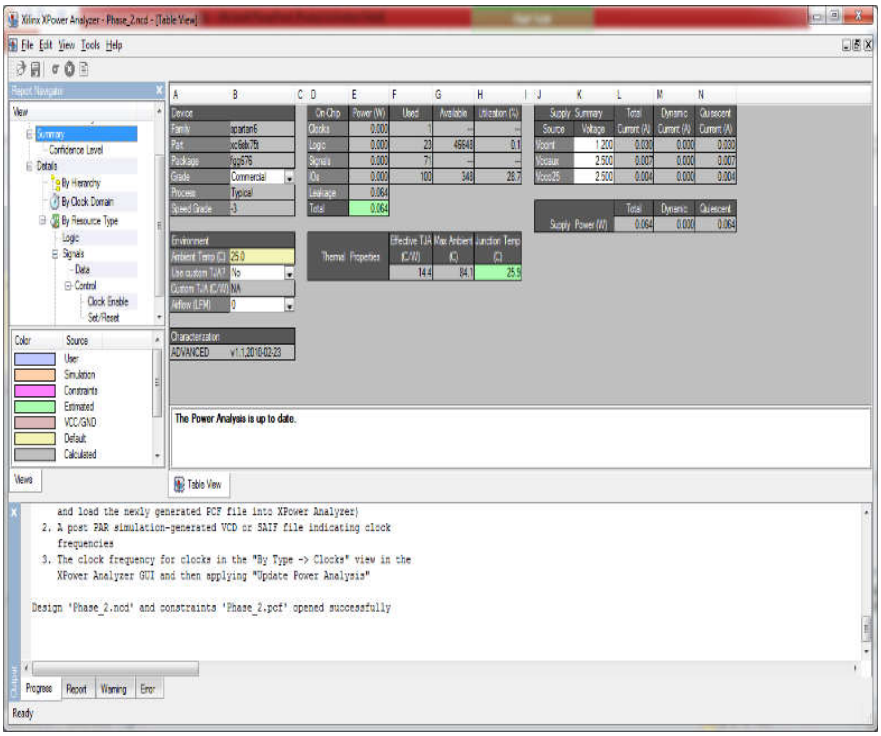

Figure 13 Stand alone Testing based 3d-MRAM Controller with MRAM Power Consumption:28.8%

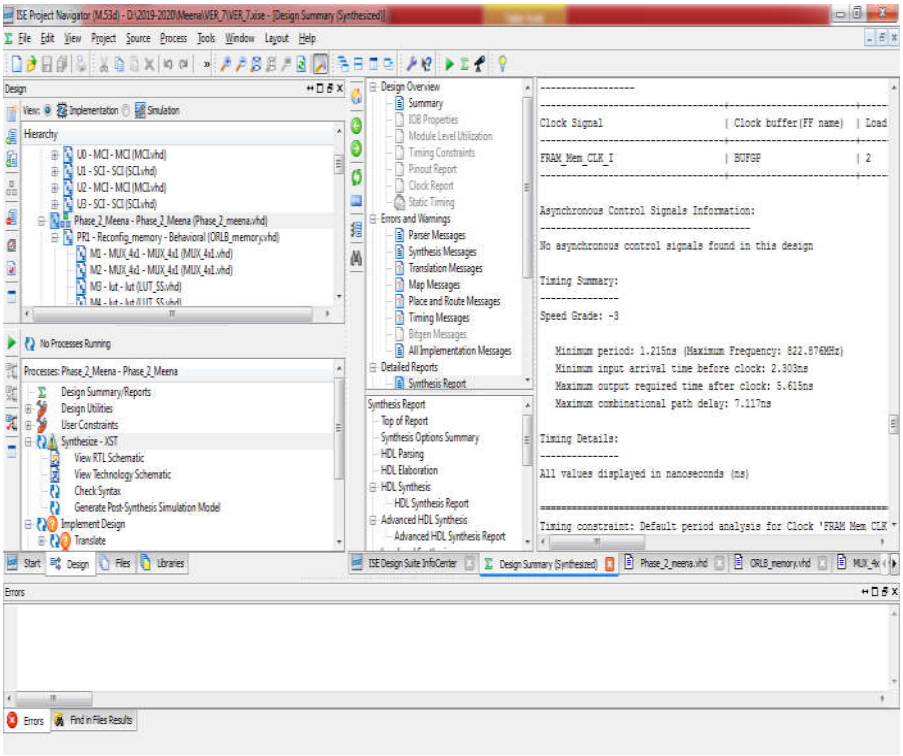

Figure 14 Reconfigurable Memory Latency: 1.215ns

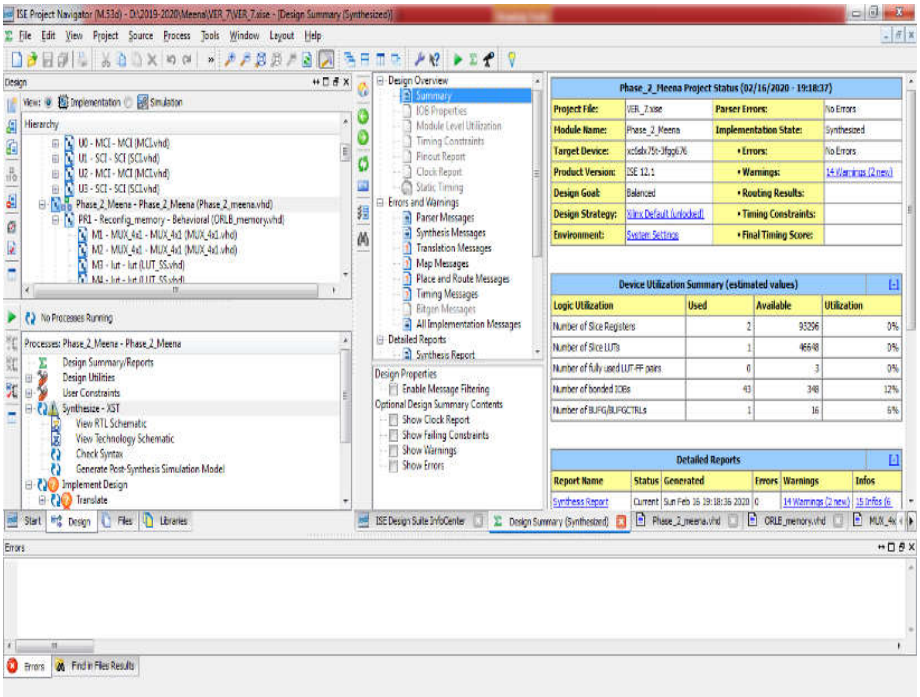

Figure 15 Reconfigurable Memory Area: 2

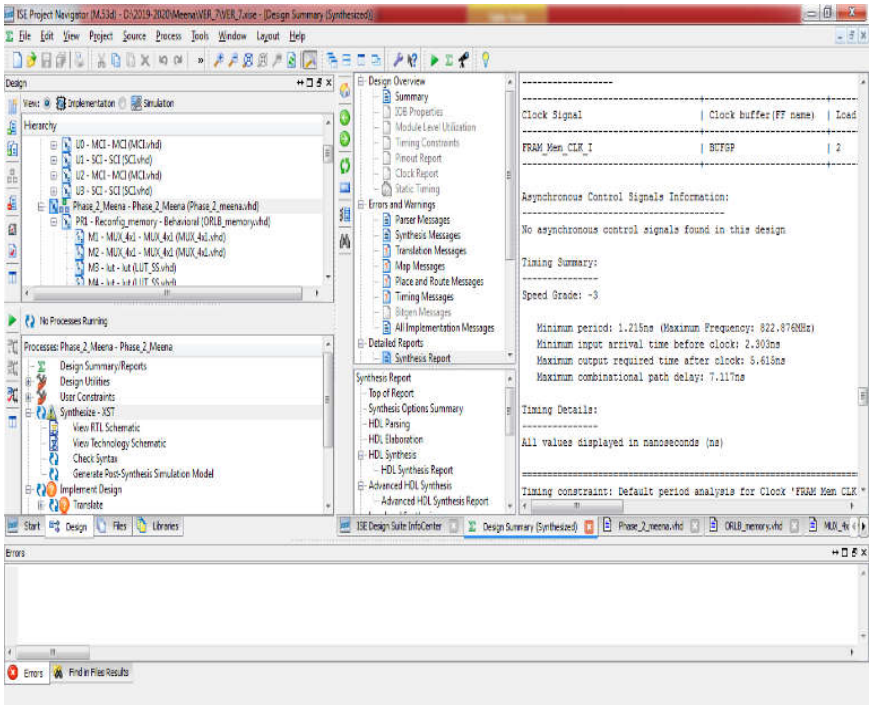

Figure 16 Reconfigurable Memory Speed: 822.876MHz

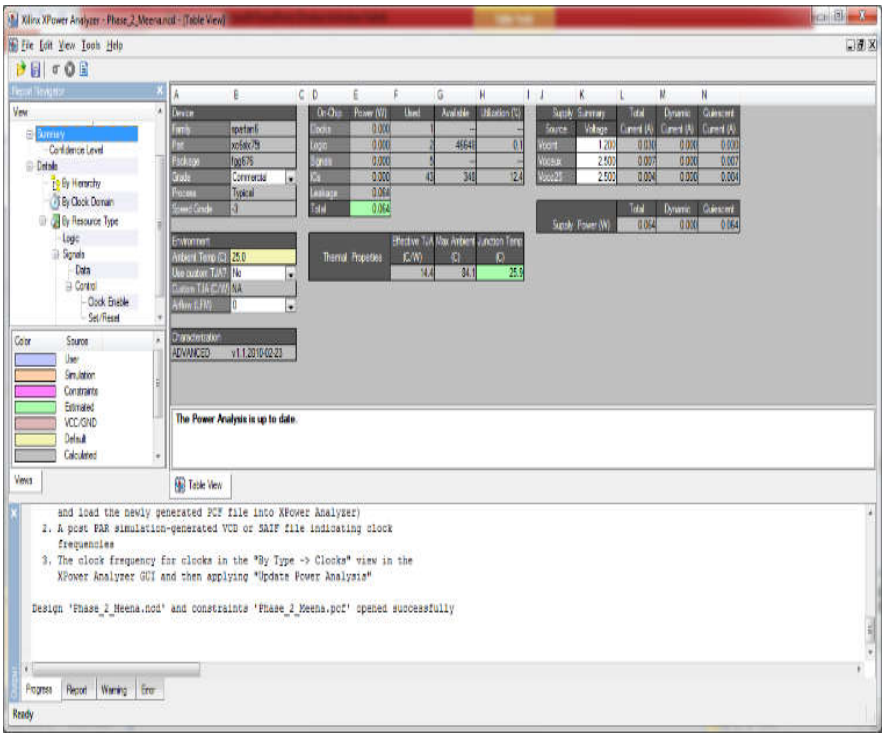

Figure 17 Reconfigurable Memory Power: 12.5 % (0.064)

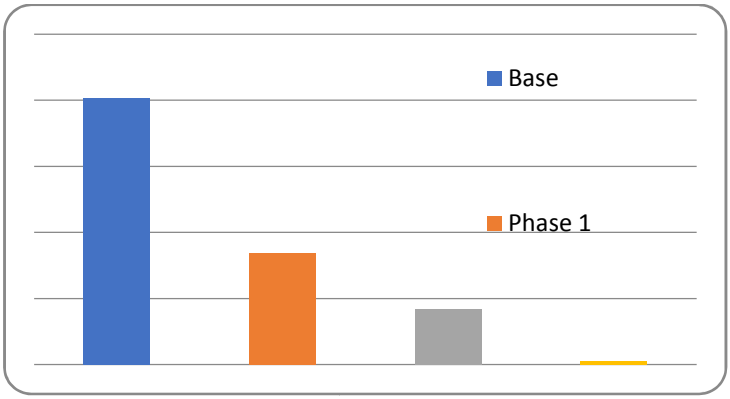

Figure 18 Performance Metric (Area)

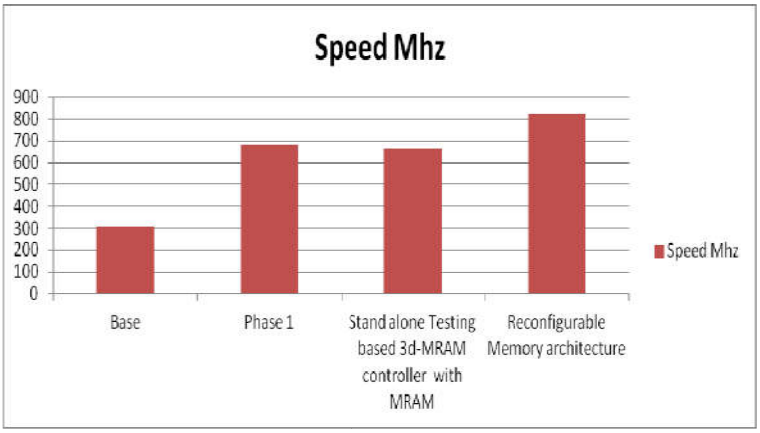

Figure 19 Performance Metric (Speed)

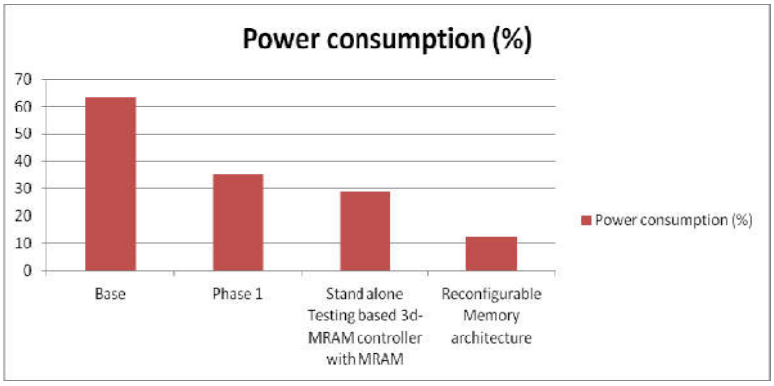

Figure 20 Performance Metric (Power Consumption)

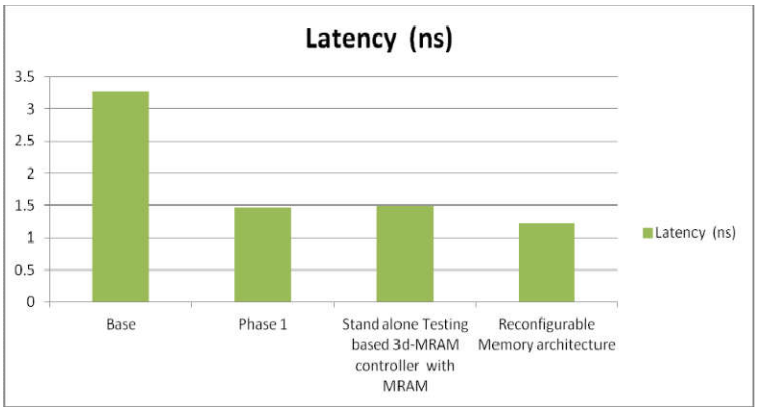

Figure 21 Performance Metric (Latency)

Comparison Table for Performance Analysis

Table 1 Performance Analysis Comparison

	Area (%)	Speed (MHz)	Power Consumption (W)	Delay (secs)
Base System	**202** **202**	**306.208**	**63.3** **63.3**	**3.266**
Proposed System	84	680.156	35.2	1.470

The above comparison table shows the various parameter metrics such as Area, Speed, Power and Delay respectively. While comparing both Base system and proposed system, the Proposed is more efficient.

Conclusions

The properties of five manufactured SCMs are presented to illustrate trade-offs available to tune performance for leakage power, area cost, robustness, and access time. Lowest leakage power is achieved using a D-latch as storage element that has stacked transistors with longer channels. Using area dense latch architecture with fewer transistors and 3-state drivers as read-logic results in the lowest area cost.

The D-latch has the highest static noise margin, and therefore, offers the lowest retention voltage. Implementing the read-logic with CMOS mixes improves the read access performance over 3-state driver based read-logic

The main objective in designing the cell by using Magnetic Random Access Memory (MRAM) is to reduce the total power consumption and data reliability. Since the MRAM is the non-volatile memory so in the absence of power supply also it provides reliability, and it consumes less amount of input supply voltage for read and write operation.

Furthermore, faster GP transistors improve access-time at a cost of leakage power increase. A flexible memory is designed by using an SCM instead of an SRAM macro, e.g., allowing a change of the number of read/write ports in the RTL code.

Furthermore, minimal engineering effort is required to change the performance properties of the SCM, i.e., replacing the storage element with a latch optimized for area cost, leakage power or access time. As an example, a single redesigned latch makes the area dense dual bit pass-latch push the area break-even point between SCMs and full-custom sub-VthSRAMs to 2 kb for single-port SRAM and 4–6 kb for dual-port SRAM.

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