21 LEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES USING PV RENEWABLE ENERGY SOURCE

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Abstract
An asymmetrical type of multilevel inverter for generating 21 voltage levels has been proposed in this paper. An asymmetrical multilevel inverter topology with PWM techniques using microcontroller with driver circuit and each panel of conventional PV voltage source added with multilevel inverter structure by additional switch and voltage source to obtain high voltage level. The objective of this project is to enhance the voltage level at the output with reduced number of switches. To improve the output voltage level. The advantage of proposed topology is to reduce the circuit complexity and also reduced numbers of switches, gate driver circuits, lower EMI and less Harmonic distortion in the inverter output voltage. The converter topology uses the midpoint voltage of the dc link to provide two more output voltage levels, decreasing switching power losses and EMI. The performance results of proposed 21-Level Asymmetrical multilevel Inverter are shown using MATLAB/SIMULINK software. The conventional control methods are mainly restricted to the direct and indirect control of the inverter.
Keywords*: Asymmetrical model, Multilevel inverter, Pulse width modulation, Photovoltaic cell.*

Introduction

Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also improves the performance of the whole system in terms of harmonics, dv/dt stresses, and stresses in the bearings of a motor. Referring to the literature reviews, the multilevel inverter (MI) with separated DC sources is clearly the most feasible topology for use as a power converter for medium & high power applications due to their modularization and extensibility. As a preliminary study the thesis examined and compared the most common multilevel topologies found in the published literature. Starting from the essential requirements, the

Different approaches to the construction of multilevel inverter are explained and compared. In particular, aspects of total harmonic distortion (THD) and modulation which are required or desirable for multilevel converters are discussed. Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance, and so on. For a medium voltage grid, it is troublesome to connect only one power semiconductor switches directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations such as laminators, mills, conveyors, pumps, fans, blowers, compressors, and so on. As a cost effective solution, multilevel converter not only achieves high power ratings, but also enables the use of low power application in renewable

energy sources such as photovoltaic, wind, and fuel cells which can be easily interfaced to a multilevel converter system for a high power application.

The most common initial application of multilevel converters has been in traction, both in locomotives and track-side static converters [4]. More recent applications have been for power system converters for VAR compensation and stability enhancement [5], active filtering [6], high-voltage motor drive [3], high-voltage dc transmission [7], and most recently for medium voltage induction motor variable speed drives [8]. Many multilevel converter applications focus on industrial medium-voltage motor drives [3, 9], utility interface for renewable energy systems [10], flexible AC transmission system (FACTS) [11], and traction drive systems [12]. The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two-level high-voltage and large-power inverters have been designed with series connection of switching power devices such as integrated gate bipolar transistors(IGBTs), because the series connection allows reaching much higher voltages. However**,** the series connection of switching power devices has big problems [13]**,** namely, non equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices. As alternatives to effectively solve the above-mentioned problems, several circuit topologies of multilevel inverter and converter have been researched and utilized. The output voltage of the multilevel inverter has many levels synthesized from several DC voltage sources. The quality of the output voltage is improved as the number of voltage levels increases, so the quantity of output filters can be decreased. The concept of multilevel converters has been introduced since 1975. The multilevel inverter was first proposed in 1975 [14]. Subsequently, several multilevel converter topologies have been developed [16]. Although the multilevel inverter was invented earlier, its application did not prevail until the mid. The advantages of asymmetric multilevel inverters were prominent for motor drives and utility applications. The 21 inverter has drawn great interest due to the great demand of medium-voltage high-power inverters. The 21 level inverter is also used in regenerative-type motor drive applications [20, 21]. Recently, some new topologies of multilevel inverters have emerged.

Multilevel Inverter

In Proposed system, twenty one level inverter was obtained from less number of switches has been implemented in existing system. This unit produces a staircase waveform with positive polarity. It is connected to a single phase full-bridge converter, which particularly alternates the input voltage polarity and provides positive or negative staircase waveform at the output. Proposed System consists of 4 solar panel of renewable Energy sources and twelve switches of Multilevel Inverter and H-Bridge inverter. The gate signals are provided by proper switching (coding) sequences using PWM logic embedded MATLAB function. Voltage and current rating of the switches play an important role in inverters.

In this topology, current through all the switches are equal with the rated load current. This converter architecture, known as the H6 bridge, was originally developed in [22], in combination

with a suitable PWM strategy, in order to keep constant the output common-mode voltage in case of a transformer less inverter for photovoltaic applications. With the same purpose, another PWM strategy for the H6 bridge was developed in [23] and [24]. In this paper, this converter structure is used to obtain a twenty one -level grid-connected converter for single-phase applications. In steady-state conditions, due to the low voltage drop across the inductance *L* of the output filter, the output voltage of the converter has a fundamental component very close to the grid voltage. The frequencies of these two voltages are identical, whereas the amplitude and their phase displacement are only slightly different. Depending on the modulation index value, the power converter will be driven by different PWM strategies and the output voltage levels of the power converter will be different. The comparison of multilevel inverter and conventional inverter as shown in Table 1.In each solar panel has two switches and which operates the positive semi period and negative semi period the switched transistors such as T1is ON and T2 is OFF. In T3 is ON and T4 is OFF commutates at the switching frequency. In finally the switching of the transistor of multilevel inverter generate either only positive or negative period of 21 level output voltage. Each inverter is able to generate three output voltage levels like +Vdc, -Vdc and 0.

Phase voltage (m) = 2n+1

the output signals is given to the H-Bridge inverter and which is operated also ON and OFF operation like inverter which produce proper positive and negative period of 21 level inverter of output voltage and also generate the load voltage and load current which is produced by using RL load. The gate a signal of switches takes from embedded MATLAB with PWM is used.

Table: 1 Comparison of Conventional Inverter and Multilevel Inverter

Conventional Inverter	Multilevel Inverter
Higher THD in output voltage	Low THD in output voltage
More switching stresses on devices	Reduced switching stresses on devices
Not applicable for high voltage applications	Applicable for high voltage applications
Higher voltage levels are not produced	Higher voltage levels are produced
Since dv/dt is high and the EMI from system is high	Since dv/dt is low and the EMI from system is low
Higher switching frequency is used and hence switching losses is high	Low switching frequency can be used and hence reduced switching losses

Asymmetrical Multilevel Inverter

This proposed system presents a new topology of multilevel inverter which uses less number of switching devices(twelve switches).In level inverter used only eight switches(S1,S2.....S8) are operated at ON and OFF operation and to generate only 21 level of positive output voltage. Then another four switches (S9, S10....S12) are used in H-Bridge inverter and it finally produces proper 21 level output voltage. In proposed system of 21 level inverter with reduced number of switches using PV source is shown in fig 1. It exhibits several attractive features such as less components, simple circuit, and modular structure. In proposed work, a method is used to compute the switching

angles for a multilevel converter. Harmonic analysis is done on twenty one levels by using capacitor based cross switched multilevel inverter. The proposed circuit generates a high-quality output voltage waveform and harmonic components of output voltage are low.

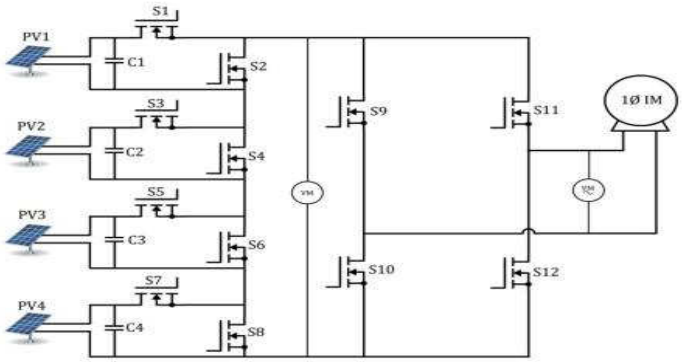

Fig.1: Asymmetrical H-Bridge Multilevel Inverter

A. Solar Panel

The proposed system consists of four solar panel (one PV panel is produced 50 V) and the one solar panel which connects two auxiliary switch of level inverter in series combination. It is connected with parallel combination of other solar panel and finally the two terminals of four solar panel which connects to the H-bridge inverter. The capacitor adder is connected between two terminals of solar panel. In solar panel of simulation circuit is shown in fig 2.

Fig.2: Solar panel

B. H-Bridge Inverter

The H-bridge inverter consists of four switches and it should perform cross switched type o turn on and turn off operation in switches. The inverter is used to convert simultaneously ac voltage to pure multilevel output voltage (ac voltage level) and the all type of switches get gate signals from PWM logic embedded mat lab function. In H-Bridge inverter of simulation circuit is shown in fig 3. Finally which inverter produces 200 V output voltages (21 level output voltage).

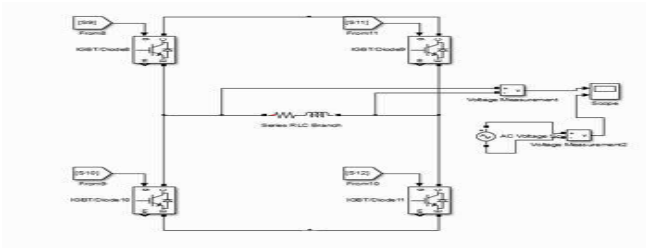

Fig.3: H-Bridge inverter

C. MATLAB Function

The MATLAB function consists of PWM logic embedded system and the gate signals of mat lab function are mainly based on coding process in mat lab. A switching sequence of coding operation for H-Bridge inverter and multilevel inverter is shown in table 2 and 3.It coding function which included the both H-bridge inverter and multilevel inverter operation. If the PWM signals go to the both type of inverter switches as a gate signals such as 8 auxiliary switches of multilevel inverter (S1, S2, S3, S4, S5, S6, S7and S8) and 4 H-bridge switches of inverter (S9, S10, S11 and S12).In simulation of mat lab function circuit is shown in fig 4.

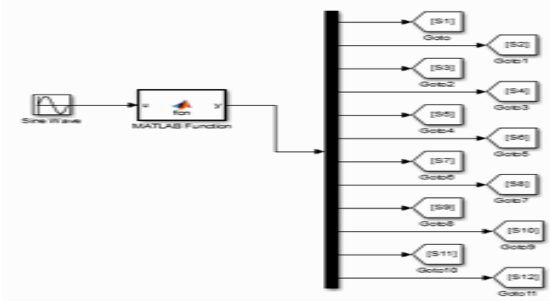

Fig.4: MATLAB Function Circuit

Table: 2 Switching Sequences of H-Bridge inverter

If u>0 (voltage)		If not u>0 (voltage)	
S9	1	S9	0
S10	0	S10	1
S11	0	S11	1
S12	1	S12	0

Table: 3 Switching Sequences of level inverter

Switching Sequence	a< 9	a<= 18	a<=27	a<=36	a<=45	a<=54	a<=63	a<=72	a<=81	a<=90	a>90	Not a>90
S1	0	1	0	1	0	1	1	0	1	0	1	0
S2	0	0	1	0	1	0	0	1	0	1	0	0
S3	0	0	1	1	0	0	1	0	0	1	1	0
S4	0	1	0	0	1	0	0	1	1	0	0	0
S5	0	0	0	0	0	0	1	1	1	1	1	0
S6	0	1	1	1	1	1	0	0	0	0	0	0

S7	0	0	0	0	1	1	0	1	1	1	1	0
S8	0	1	1	1	0	0	1	0	0	0	0	0

Circuit Operation

Control Circuit

A. Microcontroller Unit

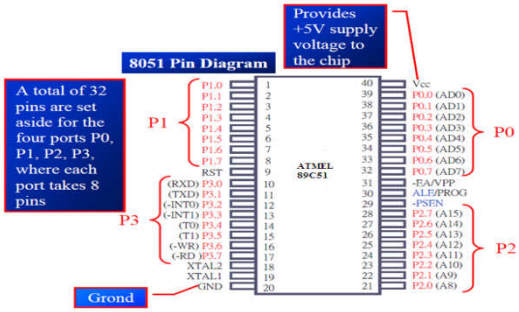

Fig.5: ATMEL 89C51 pin

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4 Kbytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51Ô instruction set and pin out. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer.

By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications. The AT89C51 provides the following standard features: 4 Kbytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes.

Table: 4 Showing the features of AT89C51

Part Number	AT89C51
ROM	4K
RAM	128 bytes
I/O Pins	32
Timers	2
Interrupts	6
Vcc	5 V
Packaging	40

B. Driver Unit

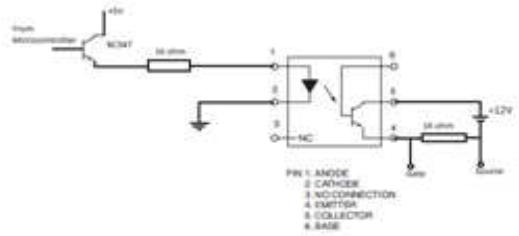

Fig: 6 Schematic of MCT2E

In contrast to bipolar transistors, MOSFETs do not require constant power input, as long as they are not being switched on or off. The isolated gate-electrode of the MOSFET forms a capacitor (gate capacitor), which must be charged or discharged each time the MOSFET is switched on or off. As a transistor requires a particular gate voltage in order to switch on, the gate capacitor must be charged to at least the required gate voltage for the transistor to be switched on. Similarly, to switch the transistor off, this charge must be dissipated, i.e. the gate capacitor must be discharged.

When a transistor is switched on or off, it does not immediately switch from a non-conducting to a conducting state; and may transiently support both a high voltage and conduct a high current. Consequently, when gate current is applied to a transistor to cause it to switch, a certain amount of heat is generated which can, in some cases, be enough to destroy the transistor. Therefore, it is necessary to keep the switching time as short as possible, so as to minimize switching loss. Typical switching times are in the range of microseconds. The switching time of a transistor is inversely proportional to the amount of current used to charge the gate. Therefore, switching currents are often required in the range of several hundred mill amperes, or even in the range of amperes. For typical gate voltages of approximately 10-15V, several watts of power may be required to drive the switch. When large currents are switched at high frequencies, e.g. in DC-to-DC converters or large electric motors, multiple transistors are sometimes provided in parallel, so as to provide sufficiently high switching currents and switching power.

The switching signal for a transistor is usually generated by a logic circuit or a microcontroller, which provides an output signal that typically is limited to a few mill amperes of current. Consequently, a transistor which is directly driven by such a signal would switch very slowly, with correspondingly high power loss. During switching, the gate capacitor of the transistor may draw current so quickly that it causes a current overdraw in the logic circuit or microcontroller, causing overheating which leads to permanent damage or even complete destruction of the chip. To prevent this from happening, a gate driver is provided between the microcontroller output signal and the power transistor.

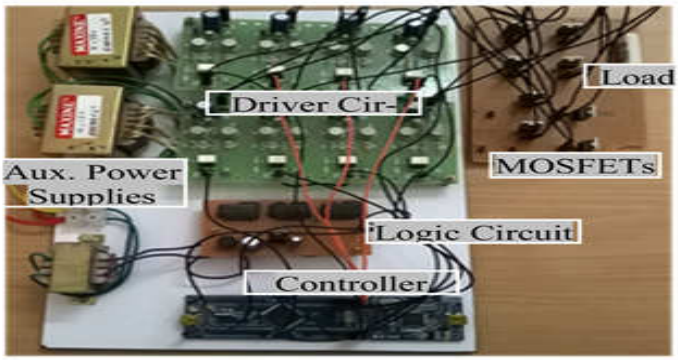

Fig.7: Hardware kit

Results

A. **Output Voltage Waveform of Solar Panel**

The output voltage value of proposed solar panel operation which has four solar panel (cell) circuits is around 80 the output voltage waveform of solar panel is shown in fig 5.

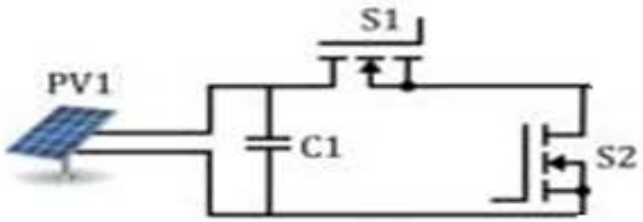

Fig.8: Basic Unit of proposed inverter

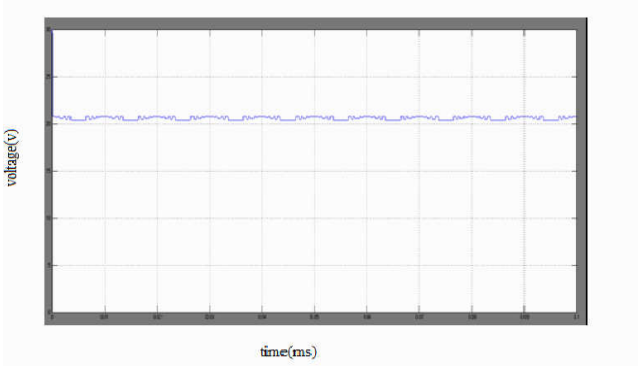

Fig.9: Output voltage of solar panel

B. **Output Voltage Waveform of 21level Inverter**

The output voltage value in proposed circuit is around 200 V. It is across the load. If the output voltage of both system is overall same but in proposed system has less number of switches will be used for generating 21 levels output voltage is shown in,fig.6.

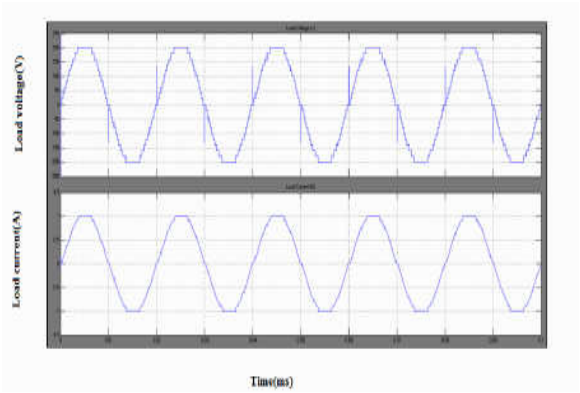

Fig.10: 21 level output voltage

C. **Output Value of Total Harmonic Distortion (Thd %)**

The output value of total harmonic distortion (THD) in proposed system is around 2.96 % is shown in fig 7 by using FFT analysis. If the value of THD is based on output voltage of 21 level inverter (act as input value) and which total harmonic Value is reduced as compared to existing system. Multilevel inverters also have several advantages like reduced total harmonic distortion (THD) as compared to existing system operation. Compared to cascaded multilevel inverter, proposed structure needs less number of components and simple control methods. The main advantages of capacitor switched multilevel inverters are good output waveform, low switching stress as compared to existing system. Higher voltages can be generated using the devices of lower rating and switching frequency can be reduced for PWM technique. The advantages of the proposed inverter are reduction of number of switches, reduction of gate driver circuits, reduction of isolated power supply unit for gate diver, lower EMI and less harmonic distortion in the inverter output voltage.

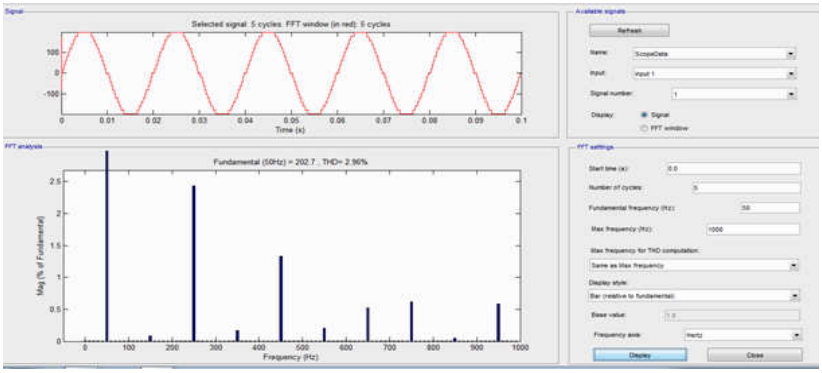

Fig.11: Total Harmonic Distortion of 21 level Inverter

Conclusion

The proposed system which utilizes four asymmetric dc sources and twelve powers switches with load. By proper switching sequence, the proposed inverter produces a 21 level output voltage with low switching losses; by operating the switches at fundamental frequency. The advantages of

the proposed inverter are reduction of number of switches, reduction of gate driver circuits, reduction of isolated power supply unit for gate diver, lower EMI and less harmonic distortion in the inverter output voltage. The computer aided simulation study has been carried out to validate the performance of proposed inverter. The proposed inverter can be recommended for distributed generators, stand alone and grid connected renewable energy power conversion applications.

References

1. E. Babaei and M. S. Moeinian, "Asymmetric cascaded multilevel inverter with charge balance control of a low resolution symmetric subsystem," J. Energy Converse Manage. vol. 51, no. 11, pp. 2272–2278, Nov. 2010A.
2. A.K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double flying capacitor multilevel converter based on modified phase shifted pulse width modulation," IEEE Trans. Power Electron., vol. 25,no. 6, pp. 1517–1526, Jun. 2010.
3. E. Babaei and S. H. Hosseini, "New cascaded multilevel inverter topology with minimum number of switches,"J. Energy Converse.Manag., vol. 50, no. 11, 2761–2767, Nov. 2009.
4. J. Rodriguez, B. Wu, S. Bernet, J. Pontt, and S. Kouro, "Multilevel voltage source converter topologies for industrial medium voltage drives," IEEE Trans. Ind. Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
5. H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium voltage multilevel converters—State of the art, challenges and requirements in industrial applications," IEEE Trans. Ind. Electron, vol. 57, no. 8, pp. 2581–2596, Aug. 2010.
6. J. S. Lai and F. Z. Peng, "Multilevel converters–A new breed of power converters," IEEE Trans. Ind. Applicat., vol. 32, pp. 509–517, May/June 1996.
7. Sanjaya Kumar Sahu1, D.D. Neema Dept. of Electrical Engg., Bhilai Institute of Technology, Durg, C.G., India Dept. of Electrical & Electronics Engg., Chhattisgarh Institute of Technology Rajanandgaon, C.G., India "A robust speed sensorless vector control of multilevel inverter fed induction motor using particle swarm optimization".
8. Arun Rahul Sanjeevan, R. Sudharshan Kaarthik, K. Gopakumar, P.P. Rajeevan, Jose I. Leon3,Leopoldo G. Franquelo3 "Reduced common-mode voltage operation of a new seven-level hybrid multilevel inverter topology with a single DC voltage source" ISSN 1755-4535 10.1049 .2015.
9. R.Rajkumar, K.Ramanathan, M.Venkatesh Kumar "Review On Various Multilevel Inverter Topologies For Renewable Energy Sources" International Journal of Applied Engineering Research, ISSN 0973-4562 Vol. 10 No.4 (2015).
10. C.Dhanamjayulu and Y. Suresh School of Electrical Engineering, VIT University, Vellore, India "Performance Verification of Novel Cascaded Multilevel Inverter (CMLI)" World Applied Sciences Journal 33 ,220-228, 2015 ISSN 18184952 ,IDOSI Publications, 2015.
11. Manoj Kumar, Mamta Singh "An Improved PSO Based Selective Harmonic Elimination in Multilevel Inverter for Performance Enhancement of Induction Motor Introduction" 2015 IJEDR | Volume 3, Issue 2 | ISSN: 2321-9939.

12. T. Sankarbalaji and Dr Y V Siva Reddy, “A Novel Cascaded Multilevel Inverter Using MCPWM With Reduced Harmonics”, RASET-2015 IJERST.
13. Ankita Rewar, A.K. Pathak “Analysis of Performance of Multilevel Cascaded Inverter” ISSN: 2278 – 909X International Journal of Advanced Research in Electronics and Communication Engineering (IJARECE) Volume 4, Issue 5, May 2015.
14. Ata Ollah Mokhberdoran, Mohammadreza Jannati Oskuee “Multilevel hybrid cascade-stack inverter with substantial reduction in switches number and power losses” 2015.
15. N.Sivakumar, A.Sumathi and R. Revathy World Engineering & Applied Sciences Journal “THD Analysis of a 13 Level Asymmetric Hybrid Cascaded Multilevel Inverter for Industrial Applications ISSN 2079-2204,IDOSI Publications, 2015.