PERFORMANCE ANALYSIS OF PWM CONTROLLED SINGLE PHASE QUASI CASCADED Z SOURCE MULTILEVEL INVERTER

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Abstract
In this paper presents a quasi-cascaded z source multilevel inverter. Owing to features of multilevel converter such as low THD, low EMI which has been recommended for different applications. The proposed inverter topology have the advantages of simple structure, reduction of passive component requirements which reduce the cost, size and weight of the inverter. In this inverter, a capacitor with low voltage rating is added to remove the offset voltage in output waveform. In addition phase shift PWM technique is used to improve the power quality and efficiency of the inverter topology. This paper designates the five level quasi cascaded z-source multilevel inverter and describe the operating principle, circuit diagram, THD evaluation using the MATLAB simulation tool.

Introduction

Multilevel inverters have drawn many attentions from researchers which is their advantage over the conventional three level pulse width modulation (PWM) inverters. The advantages of the multilevel inverters are being followed: improved quality output waveforms with low total harmonic distortion (THD), smaller filter size and low electromagnetic interface (EMI). Three generalized multilevel inverter topologies are: flying capacitors, neutral point clamped (NPC), and cascaded H-bridge (CHB) inverters. Among the topologies discussed the CHB inverter has an unique advantage in its modularity and its contribution of high power. These advantages make the Cascaded H-bridge inverter an attractive option for many applications such as uninterruptible power supplies (UPS), grid connected system, StatCom system, motor drive, etc. However, the traditional CHB multilevel inverter is a buck DC-AC power conversion, where the peak AC output voltage is limited by the total DC source voltages. An additional DC-DC boost converter is in demand for each type of module in the CHB topology to achieve the high AC output voltage when the DC input voltages are low. Adding DC-DC boost power converter results in low efficiency and high cost. The boost converter of DC-DC type is used to control the DC-link voltage on each H-bridge circuit.

In the CHB-qZSI, a shoot through (ST) state is used to boost voltage without any damages in the power circuit. In one switching period, the number of the single-phase qSBI is two. Therefore, the operating frequency of the inductors is two-fold the switching frequency. In the CHB-qZSI, the input DC current is continuous with lower ripple. Each module in the CHB qZSI can produce the same DC-link voltage by control the ST duty cycle. Like the CHB-qZSI, an active front end AFE-CHB inverter also and buck/boost voltage. However, the CHB-qZSI and the AFE-CHB inverter use a large number of passive elements with raising the size, cost, and weight of the power cascaded system. This project proposes a seven level inverter which uses a quasi Z source inverter with reduced components.

Advantages

1. Low shoot through duty cycle.
2. High gain output voltage.
3. Control circuit is easy.
4. Low noise in the output voltage.

Proposed Topology

The Quasi Z-Source inverter circuit differs from that of conventional quasi Z Source Inverter in LC impedance network interface between the source and inverter. Quasi Z source inverter acquires all the advantages of traditional Z Source Inverter. The basic topology of Quasi Z Source inverter. The Quasi Z Source inverter (QZSI) extends several advantages over Z Source inverter such as continuous input current, reduced components rating, and enhanced reliability. These advantages make the Quasi Z source inverter (qZSI) suitable for power conditioning in renewable energy system. A PV cell's voltage varies widely with temperature and irradiation, but the traditional voltage Source Inverter (VSI) cannot deal with this wide range without over rating of the inverter. Because of this, a transformer and or a dc/dc converter is usually used in PV applications, in order to cope with the range of the PV voltage , reduced inverter rating, and to produce desired voltage for the load or connection to the utility. This leads to a high component count and low efficiency, which opposes the goal of cost reduction. The Z Source Inverter has been reported suitable for residential PV system because of the capability of voltage boost and inversion in a single stage. Recently, four switches new topology, the quasi Z Source Inverter (qZSI), have been derived from the original ZSI Fig.3.1.

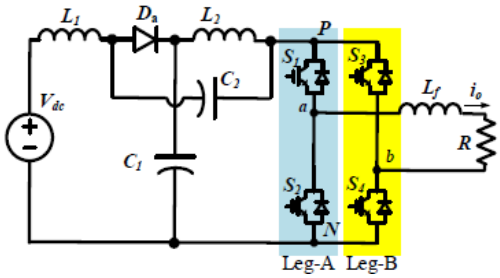

Fig. 3.1: Basic circuit of quasi Z source inverter

By using the new quasi Z-source topology, the inverter draws a constant current from the PV array and is capable of handling a wide input voltage range. It also features low component rating, and reduced source stress compared to the traditional ZSI. It is demonstrated from the theoretical analysis and simulation results that the proposed qZSI can realize voltage buck or boost and dc-ac inversion in a single stage with high reliability and efficiency, which makes it well suited for PV power systems.

The quasi Z Source inverter circuit differs a form of a DC voltage source connected along with inductor, capacitor and diode device to form a z source and also partially conductive quasi source is connected to the MOSFET switches to give the AC output voltage. Quasi Z-source inverter acquires

all the advantages of traditional Z-Source Inverter. The basic topology of Quasi Z-source inverter. The quasi Z source inverter extends several advantages over Z source inverter such as continuous input current, reduced component rating, and enhanced reality in qZSI.

Operating Principle

In the same manner as the traditional ZSI, the qZSI has two types of operational states at the dc side: the non shoot through states (the six active states and two conventional zero states of the traditional VSI) and the shoot through state (in the both switches in at least one phase conduct simultaneously). In the non shoot through states, the inverter bridge view from the dc side is equivalent to a current source. The equivalent circuits of the two states are as shown in Fig.3.2 and Fig3.3. The shoot through state is forbidden in the traditional VSI, because it will cause a short circuit of the voltage source and damage the devices. With the qZSI and ZSI, the unique LC and diode network connected to the inverter bridge modify the operation of the circuit, allowing the shoot through state. This network will effectively protect the circuit from damage when the shoot through occurs and by using the shoot though state, the quasi Z-source network boosts the dc-link voltage. The major differences between the ZSI and qZSI are the qZSI draws a continuous constant dc current from the source.

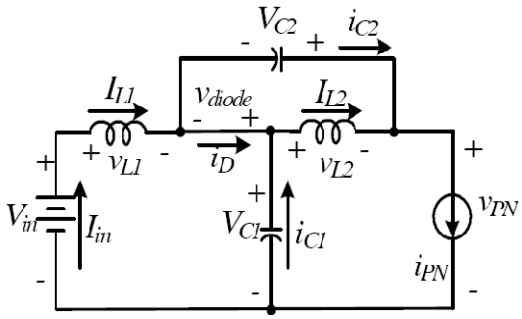

Fig. 3.2: Equivalent circuit of shoot through state

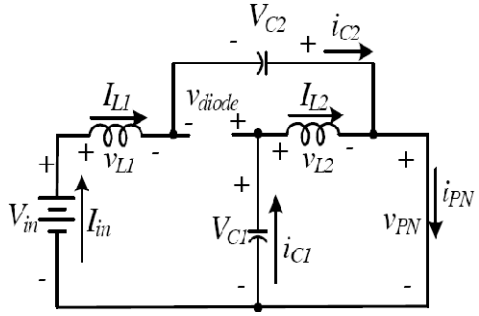

Fig. 3.3: Equivalent circuit of non shoot through state

All the voltages as well as the currents are defined in and the polarities are shown with arrows. That duration one switching cycle T, the interval of the shoot through state is T_0; the interval of nonshoot through states is T_1; thus one has $T= T_0+T_1$and the shoot through duty ratio, $D= T_0/T$. Which is a representation of the inverter during the interval of the non shoot through states T_1.

Phase Shifted Sinusoidal Pulse Width Modulation

The switches in the voltage source Fig. inverter can be turned on and off as required. In the simplest approaching, the top switch is turned on if turned on and turned off. Only once in each cycle, a square waveform and its results. However, if turned on several times in a cycle at improved harmonic profile can be achieved.

In the most straight forward implementation, generation of the desired output voltage is achieved by comparing the desired reference waveform (modulating signal) with a high-frequency triangular 'carrier' wave as depicted. Depending on whether the signal voltage is larger or smaller than the carrier waveform, either the positive or negative dc bus voltage is applied at the output. Note that all over the period of one triangle wave, the average voltage applied to the load is proportional to the amplitude of the signal (assumed constant) during this period. The resultant chopped square waveform contains a replica of the desired waveform in its low frequency components, with the higher frequency components being at frequencies of an close to the carrier frequency. Notice that the rms value of the ac voltage waveform is still equal to the dc bus voltage, and hence the total harmonic distortion is not affected by the PWM process. The harmonic components are simply shifted into the higher frequency range and are automatically filtered due to inductance in the ac system

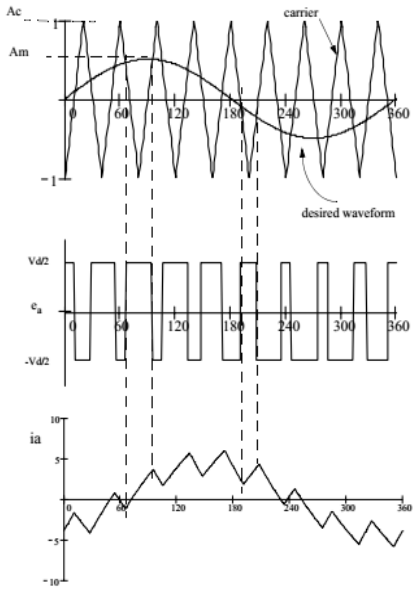

Fig. 3.4: Principal of Pulse Width Modulation

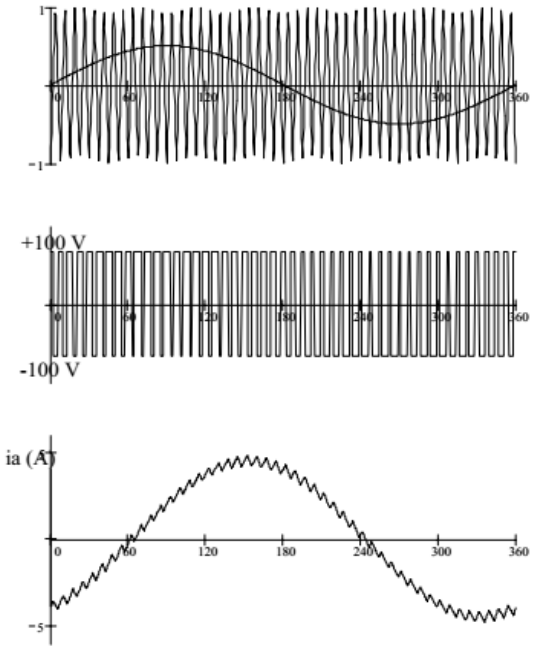

Fig. 3.5: SPWM with fc/fm = 48, L/R = T/3

Note that the process works well for m ≤ 1. For m > 1, there are periods of the triangle wave in which there is no intersection of the carrier and the signal. However, a certain amount of this "over modulation" is often allowed in the interest of obtaining a larger ac voltage magnitude even though the spectral content of the voltage is rendered somewhat poorer.

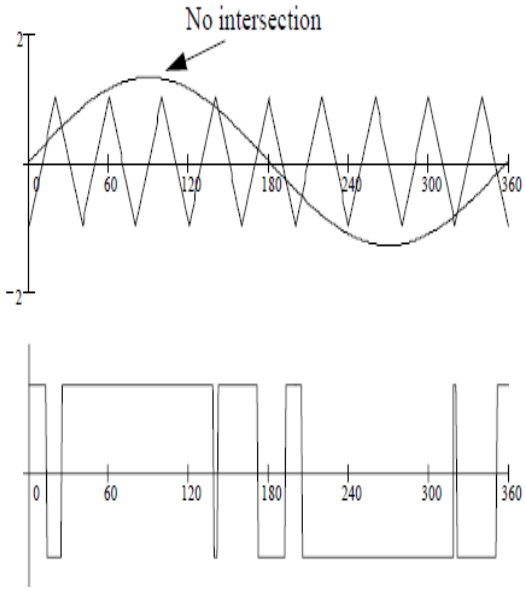

Fig. 3.6: Over Modulation

Note that with an odd ratio for fc/fm, the waveform is anti-symmetric over a 360 degree cycle. With an even number, there are harmonics of even order, but in particular also a small dc component. Hence an even number is not recommended for single phase inverters, particularly for small ratios o fc/fm.

SPWM Spectra

Although the SPWM waveform has harmonics of several orders in the phase voltage waveform, the dominant ones other than the fundamental are of order n and n±2 where n = fc/fm. This is evident for the spectrum for n=15 and m = 0.8.Note that if the other two phases are identically generated but 1200 apart in phase, the line-line voltage will not have any triplet harmonics. Hence it is advisable to choose, fc/fm = 3k, (k ∈ N), as then the dominant harmonic will be eliminated. It is evident from that the dominant 15th harmonic in is effectively eliminated in the line voltage. Choosing a multiple of 3 is also convenient as then the same

Triangular waveform has been used as the carrier form in all three phases, leading to some simplification in hardware. It is readily seen that as the (pwm (θ)) 2 = E2 where E is the dc bus voltage, that the rms value of the output voltage signal is unaffected by the PWM process. This is stringently true for the phase voltage as triple harmonic orders are canceled in the line voltage. However, the problematic harmonics are phase shifted to higher orders, thereby making filtering much easier. Often, the filtering is carried out via the natural high impedance characteristic of the load.

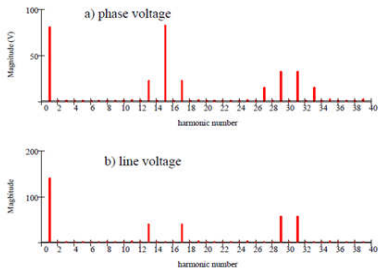

Fig. 3.7: SPWM Harmonic Spectra: n = 15, m =0.8

Proposed System

Block diagram of proposed system

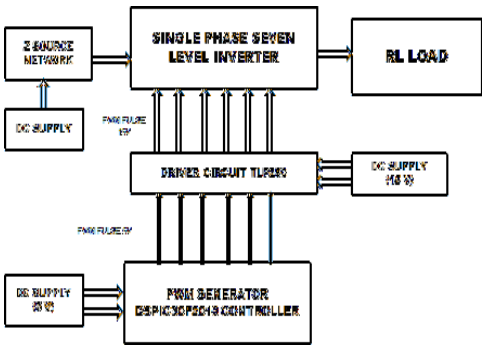

Fig. 4.1: Block diagram of proposed system

The proposed system uses a cascaded combination single phase quasi Z-source inverter topologies. This topology is used to generate a seven inverter output. Main the main blocks involved in this topology are discussed below. A quasi Z-source network which is connected to a single phase H-bridge this constitute a single module. A total of three such modules are used to produce the seven level output. The arrangement of this module is in series fashion. A PWM generator is used to produce the desired output from the inverter topology.

Circuit Diagram

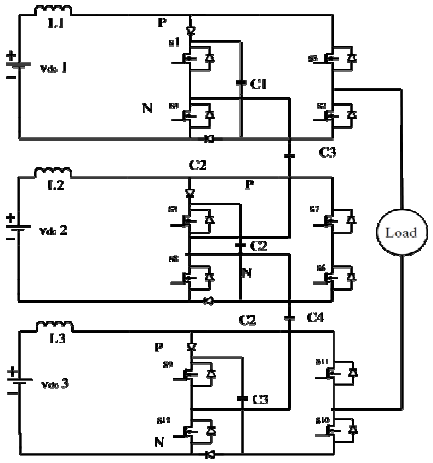

Fig. 4.2: Proposed qCHB-SLBI

The configuration of the proposed single phase quasi cascaded h-bridge seven level boost inverter is fig.4.2.The proposed inverter consists of three separate DC source, three quasi boost inverter module and capacitor filter connected in resistive load in series. Each module contains five capacitor, three boost inverter, twelve switches, and six diode. The output voltage of proposed qCHB-SLBI has seven levels.

Table.4.1 Switching scheme for seven level CMLI

S_1	S_2	S_3	S_4	S_5	S_6	S_1'	S_2'	S_3'	S_4'	S_5 ,	S_6 ,	Vab
1	0	0	1	1	0	0	1	1	0	0	1	+3 Vdc
1	0	0	1	1	0	0	1	1	0	1	0	+2 Vdc
1	0	0	1	0	1	0	1	1	0	1	0	+1 Vdc
1	0	1	0	0	1	0	1	1	0	1	0	0
0	1	1	0	0	1	1	0	1	0	0	1	-1V dc
0	1	1	0	0	1	1	0	0	1	0	1	-2V dc
0	1	1	0	0	1	1	0	0	1	1	0	-3V dc

Table: 4.1.The quasi Z source inverter boost the dc-link voltage. Comparing with the normal quasi Z source inverter, the impedance are arranged so as to form the represented structure of qZSI. The proposed Quasi Z source inverter based seven level cascaded multilevel inverter is controlled with their AC outputs transiting between the seven distinct voltages. They are: +3Vdc, +2Vdc, +Vdc, 0, -Vdc, - 2Vdc,-3Vdc. To obtain the seven levels inverter, the required switching scheme is given in Table.1. The presented qZSI is expected to performed better, since performance limitations commonly associated with dead-time delay which was avoided. The qZSI is responsible for the voltage boost up inverter. The inversion is performed by a supplying PWM signals to the switches of the circuit in a certain fashion so as to produce seven levels at the output. QZSI is a symmetrical network. The operating states of the qZSI are shoot through zero state and non-shoot through zero state. In this proposed inverter the number of bridges required is 3 hence it consists of 12 switches.
In summary, the voltage and current stress of the qZSI are shown in Table 4.1.

The stress on the ZSI is shown as well for comparison, where
M is the modulation index; is the ac peak phase voltage; P is the system power rating.
$M = T_1 / T_2\text{-}T_0$; $n = T_0 / T_1\text{-}T_0$ thus m>1; m-n=1;
$B = T/T_1 - T_0$ thus m+n=B, 1<m<B

From Table 4.2. We can find that the qZSI inherits all the advantages of the ZSI. It can buck or boost a voltage with a given boost factor. It is able to handle a shoot through state, and therefore it is more reliable than the traditional VSI. It is unnecessary to add a dead band into control schemes, which reduces the output Distortion.

Table 4.2 Voltage and Average Current of the qZSI and ZSI Network

	$v_{L1} = v_{L2}$		v_{PN}		v_{diode}	
	T_0	T_1	T_0	T_1	T_0	T_1
ZSI	mV_{in}	$-nV_{in}$	0	BV_{in}	BV_{in}	0
qZSI	mV_{in}	$-nV_{in}$	0	BV_{in}	BV_{in}	0
	V_{C1}		V_{C2}		$\hat{v}_{ln}$	
ZSI	mV_{in}		mV_{in}		$MBV_{in}/2$	
qZSI	mV_{in}		nV_{in}		$MBV_{in}/2$	
	$I_{in} = I_{L1} = I_{L2}$		$I_{C1} = I_{C2}$		I_D	
ZSI	P/V_{in}		$I_{PN} - I_{L1}$		$2I_{L1} - I_{PN}$	
qZSI	P/V_{in}		$I_{PN} - I_{L1}$		$2I_{L1} - I_{PN}$	

Proposed System

Simulation and Results

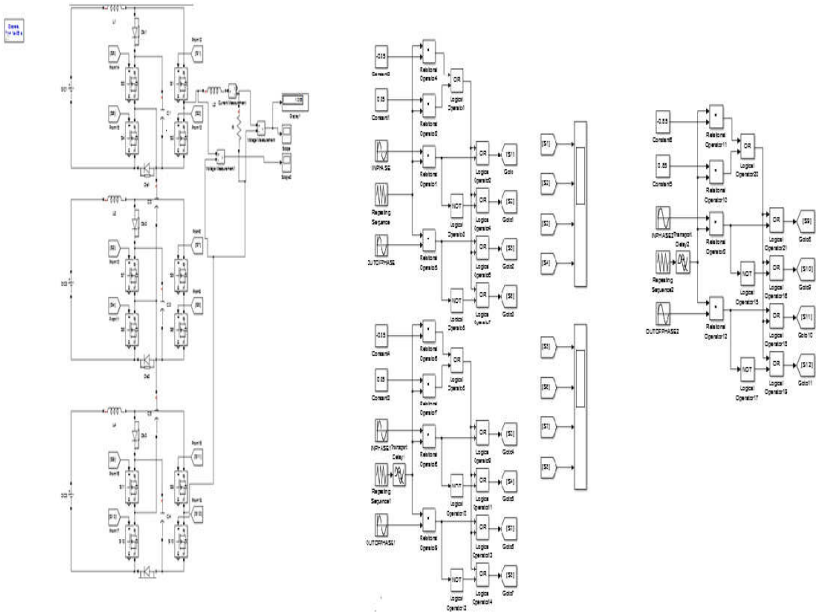

Fig: 5.1: Simulation model of proposed system

Table: 5.1 Simulation Parameters

Parameters		Values
Inverter Input voltage		50Vrms
Output Voltage		150V
Output frequency		50Hz
Capacitor		4.4e-3 F
Load	Inductor	3e-3 H
	Resistor	40 Ohms
Switching Frequency		10kHz

Output Voltage Waveform

The seven level output voltage waveform of the proposed system with amplitude 150V.

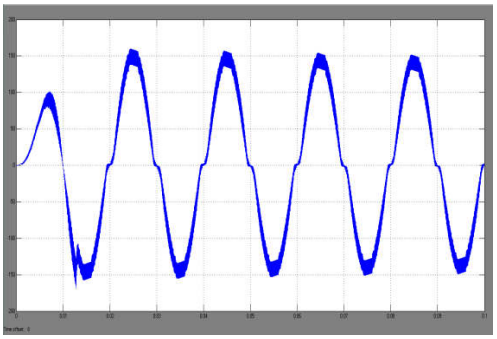

Fig. 5.2: Seven level output voltage waveform

FFT Analysis Proposed System

The Total Harmonics Distortion result of 09.44% with the proposed system.

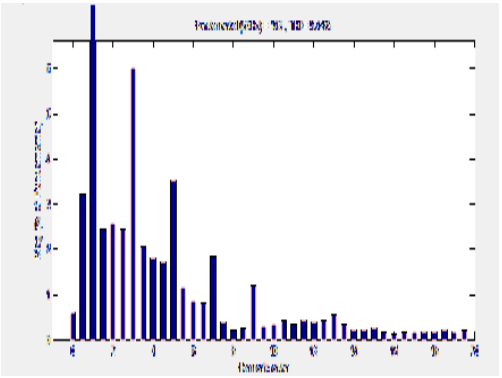

Fig. 5.3: THD result of proposed system

In this project the comparison of THD for single Phase cascaded H bridge multilevel inverter is done between 5 level and 7- level as given in the fig: 5.1. Single phase cascaded H Bridge inverters are implemented in MATLAB/SIMULINK. A MOSFET is selected as a switch. The switches are triggered at regular intervals.

Table 5.2 THD Comparison

S. No	No .of levels	THD
1	5	18.82
2	7	09.44

Conclusion

This project presents a qZSI with a new topology, which is derived from the traditional ZSI. The proposed CHB-QZSI inherits all the advantages of the ZSI and it can realize buck/boost power conversion in a single stage with a wide range of gain that is suited well for application in power generation system. The proposed qZSI has advantages of continuous input current, reduced source stress, and lower components ratings when compared to the traditional ZSI. The proposed system is able to feed good quality power into the load for a single low voltage with current THD of 09.44%. A simulation based analysis of the proposed system was done using MATLAB and effectiveness of the proposed system was evaluated by doing a comparative study with the existing system.

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